Helio X20:
The First Tri-Gear Mobile SoC with CorePilot™ 3.0 Technology

Tsung-Yao Lin, Ming-Hsien Lee, Loda Chou, Clavin Peng, Jih-Ming Hsu, Jia-Ming Chen, John-CC Chen, Alex Chiou, Artis Chiu, David Lee, Carrie Huang, Kenny Lee, TzuHeng Wang, Wei-Ting Wang, Yenchi Lee, Chi-Hui Wang, Pao-Ching Tseng, Ryan Chen, Kevin Jou

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Agenda

Tri-Gear Concept

Challenges

Key Technologies

- Tailored CPU cores for gears
- Enhanced coherent interconnect
- Hybrid scheduler
- Holistic gear allocation
- Adaptive thermal management

Achievements

Summary

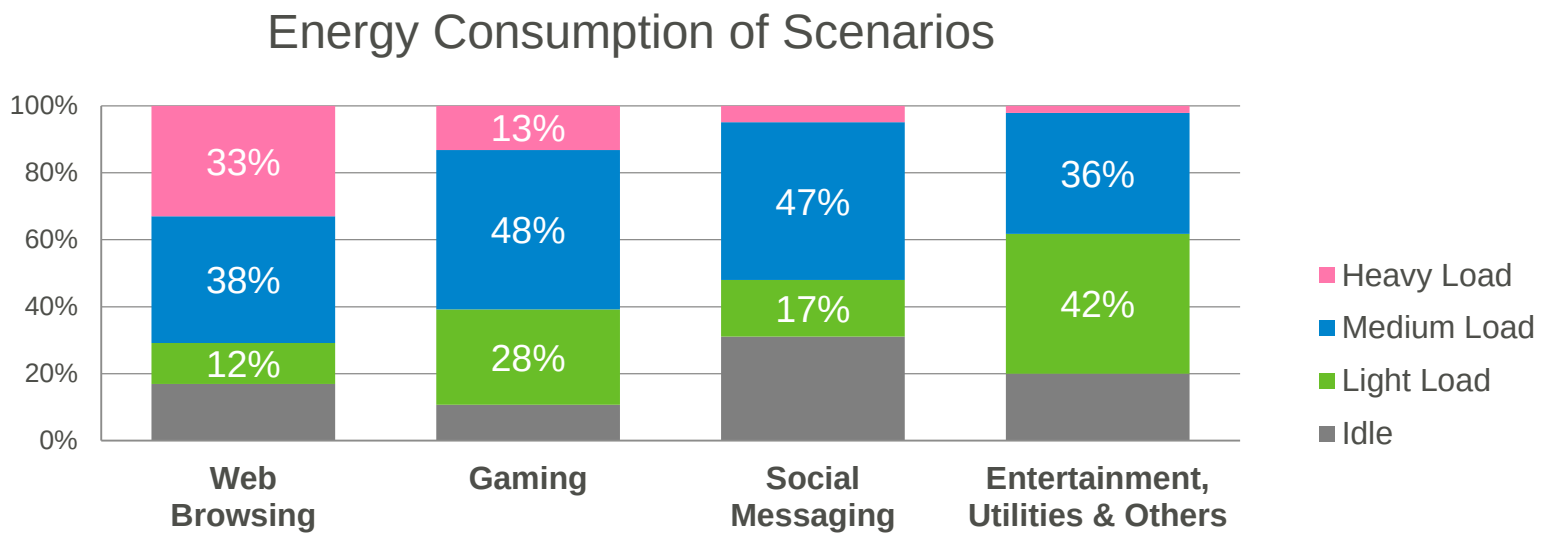
User Behavior Changed

Source: Flurry Analytics

Scenarios	Example Application	Task Load	Time Spent% Per Day (2013)	Time Spent% Per Day (2014)	Time Spent% Per Day (2015)	Changes (2014→2015)
Web Browsing	Chrome Browser	Heavy ~ Medium	20%	14%	10%	**-4%**
Gaming	Temple Run 2	Heavy ~ Light	32%	32%	15%	**-17%**
Social Messaging	Facebook	Medium	24%	28%	31%	**+3%**
Entertainment, Utilities, and others	YouTube, Mail	Medium ~ Light	24%	26%	44%	**+18%**

- **Social messaging, entertainment, and utilities (with medium to light loads) take up to 75% of user time**

Task Load Distribution of Scenarios



- **Medium load tasks are important across all scenarios (36% ~ 48%)**
- **Heavy load tasks are still important for specific scenarios**

The Dual-Gear Dilemma

Light Tasks

Medium Tasks

Heavy Tasks

LITTLE

- always-on, connected

big

- game
- multimedia

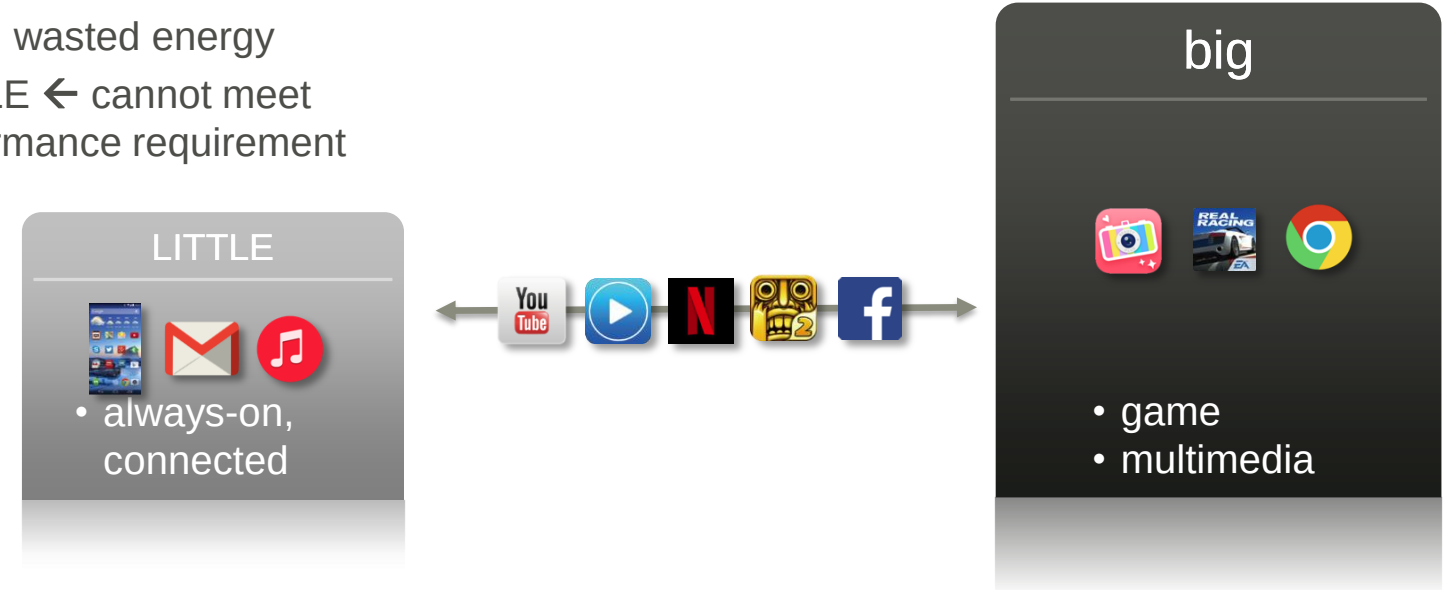
MEDIATEK

The Dual-Gear Dilemma

Light Tasks | Medium Tasks | Heavy Tasks

Execute medium load tasks on

- big → wasted energy
- LITTLE ← cannot meet performance requirement



The Dual-Gear Dilemma

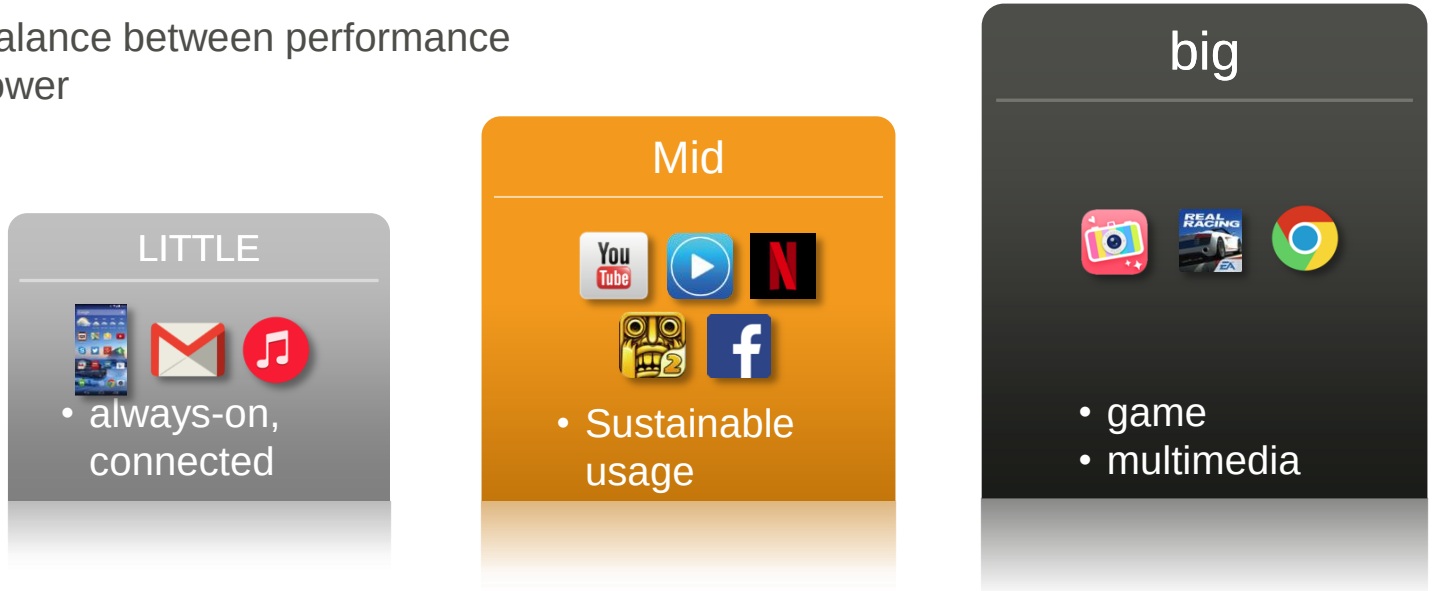
Light Tasks

Medium Tasks

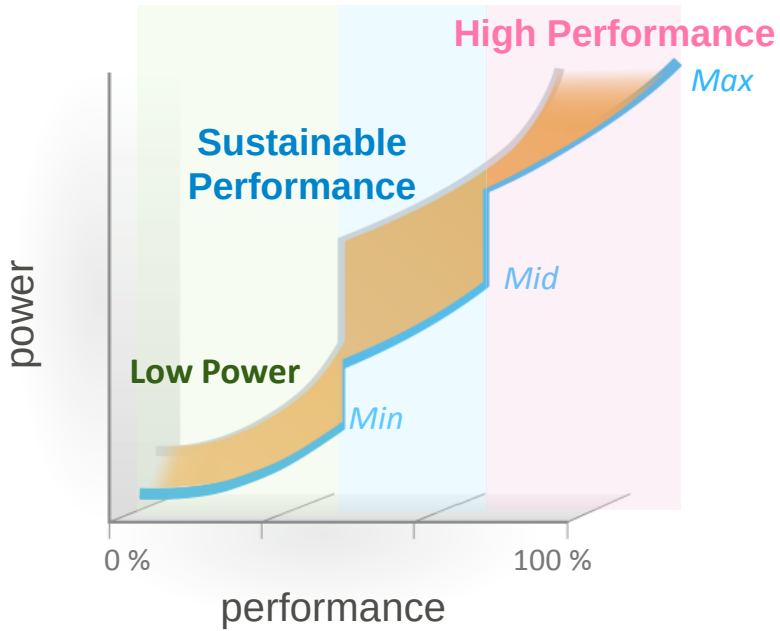
Heavy Tasks

Execute medium load tasks on

- Mid: balance between performance and power



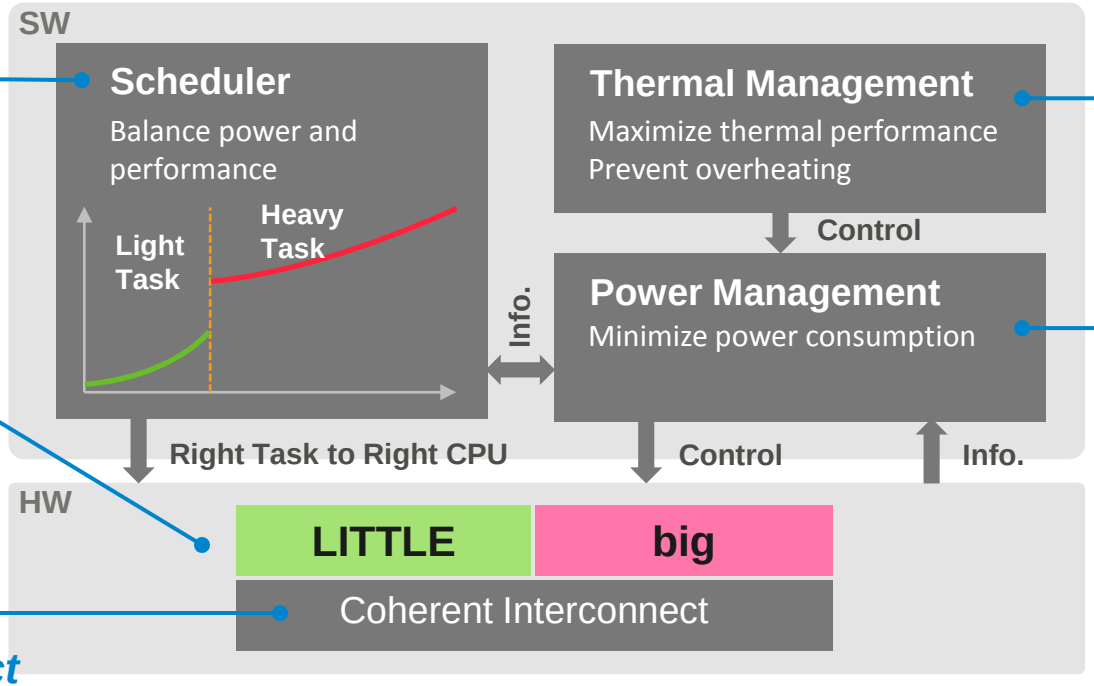
Introduction to Tri-Gear



1. New **Mid** gear introduced
2. **Min** gear goes for even lower power,
   Max gear aims for higher performance
3. Reduced power consumption
   across entire performance range

Challenges of Tri-Gear

Evolving to Tri-Gear



Revised scheduler

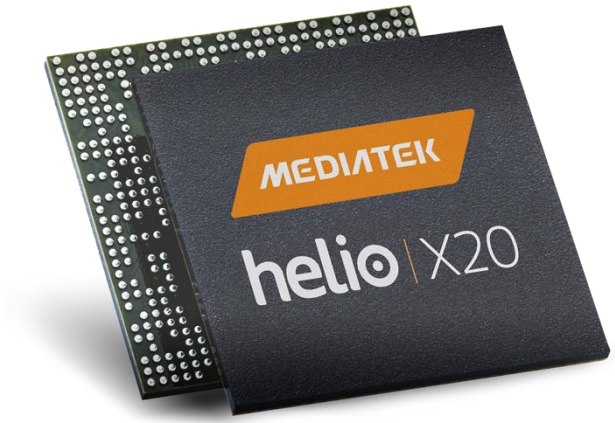
Improved thermal sensing, power budgeting

Improved gear management

Tailored processors

Enhanced coherent interconnect

Agenda



Tri-Gear Concept

Challenges

Key Technologies

- Tailored CPU cores for gears
- Enhanced coherent interconnect
- Hybrid scheduler
- Holistic gear allocation
- Adaptive thermal management

Achievements

Summary

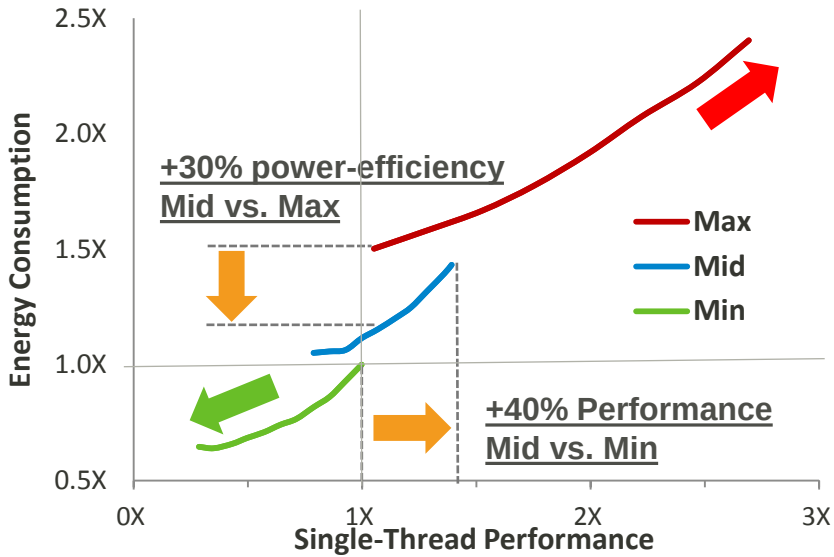
Tailored CPU Cores for Three Gears

Mid gear for efficient performance

- **+30% power-efficiency**
  - Multi-bit flip-flops optimization
  - Delicate usage of high leakage LVT cells
- **+40% performance vs. Min gear**
  - LIB and MEM optimizations

Min, Max gears extend power/performance ranges

A53	A53	A53	A53	A53	A53	A53	A53	A72	A72
1.4GHz Min				2.0GHz Mid				2.5GHz Max	



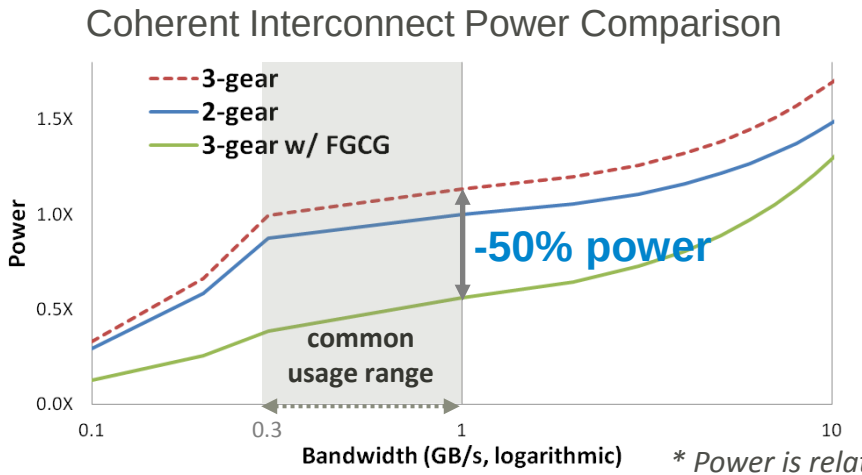
** Energy and Performance scale relative to the highest point of Min curve*

Enhanced Coherent Interconnect

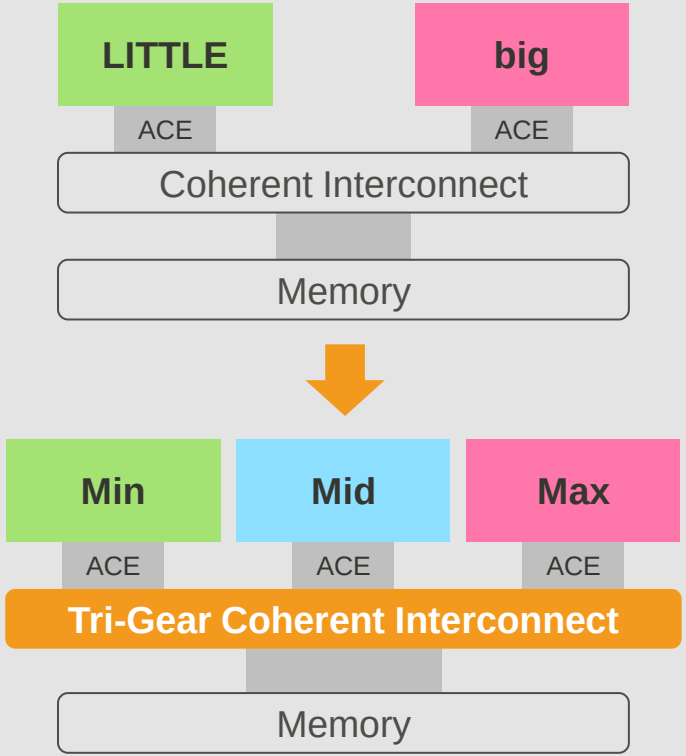
Enhanced from 2 ACE ports to 3 ACE ports

Increased logic → extra power

- ~50% power reduction by sub-module Fine-Grain Clock Gating (FGCG)



** Power is relative to 2-gear at 1GB/s*



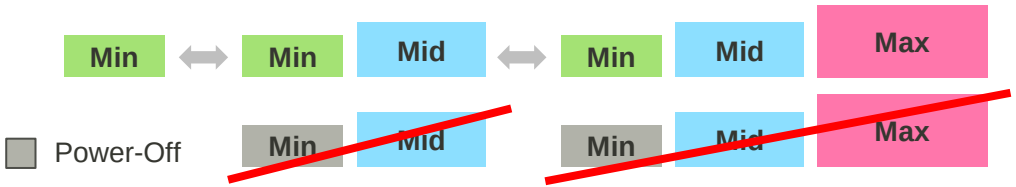
Hybrid Scheduler

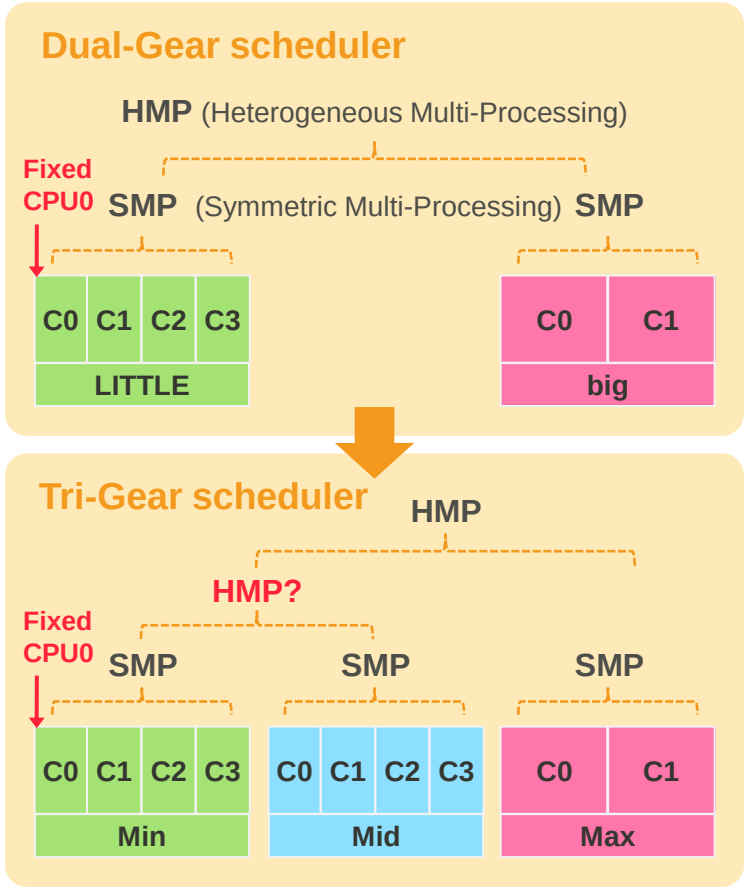
HMP Dual-Gear scheduler

- Limited to Dual-Gear
- Boot CPU is always on and cannot be migrated (Fixed CPU0)
  Typically in LITTLE → LITTLE cannot be off

Dual-level HMP scheduler for Tri-Gear?

- Might not be optimal
- Fixed CPU0 limits power saving opportunities

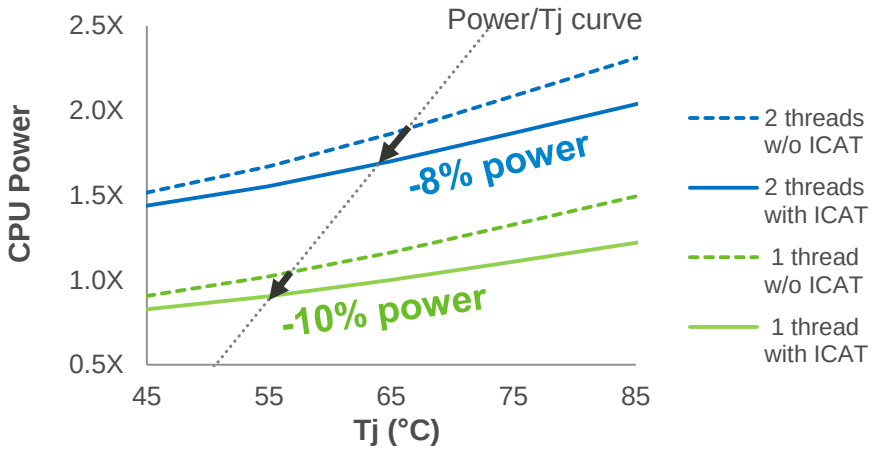




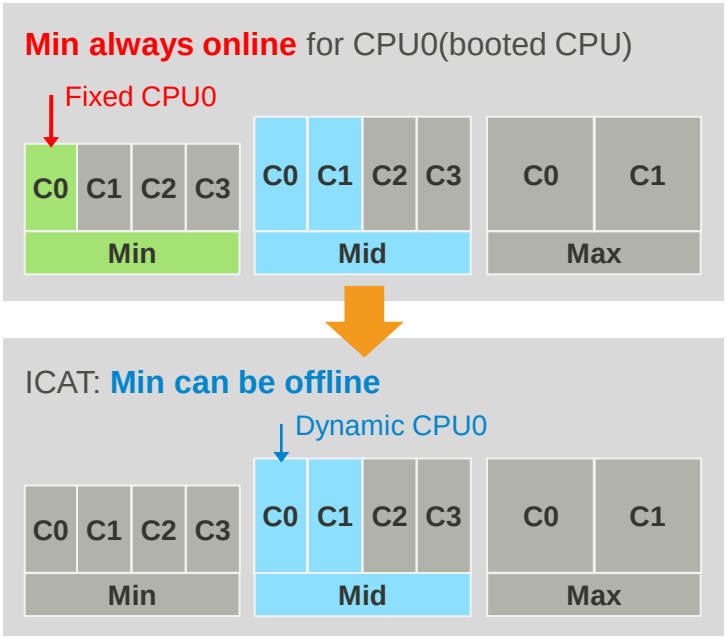
Intelligent Core Activation Technology (ICAT)

ICAT assigns CPU0 dynamically

- Min gear can be off by task migration
- **8%~10%** CPU power saved for medium load



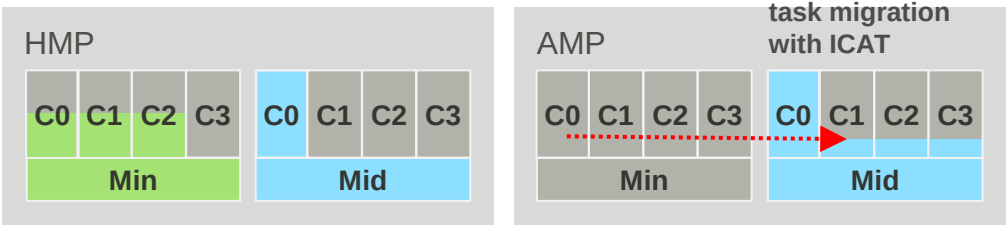
** Power is relative to 1 thread with ICAT at 65℃*



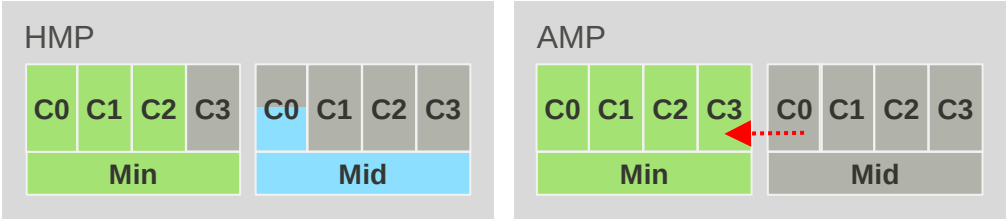
Asymmetric Multi-Processing (AMP) with ICAT

AMP: enhanced HMP with dynamic gear operation for power saving

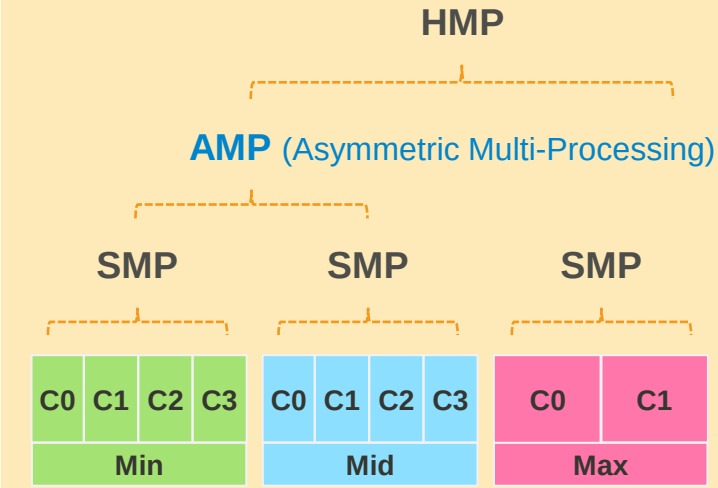
- Packing tasks to **Mid** for sustainable performance



- Packing tasks to **Min** for low power



Tri-Gear scheduler



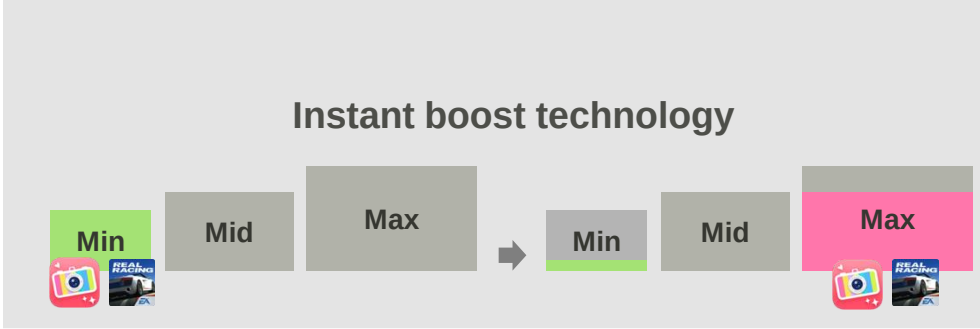
Hybrid Scheduler

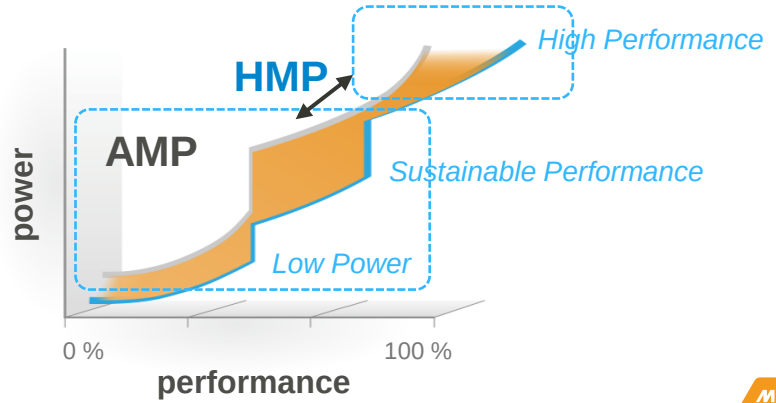
HMP for high performance

- **Instant boost technology**
  - Quick response to utilize Max for urgent or heavy tasks

Hybrid = SMP + AMP + HMP

- **Inter-gear task migration**
  - **Dynamic threshold control** for energy efficiency and responsiveness
  - **Thread-group migration** strategy to increase cluster (L2 cache) locality

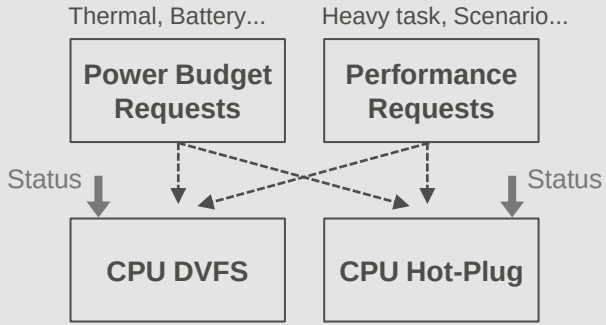




Enhanced Power Management

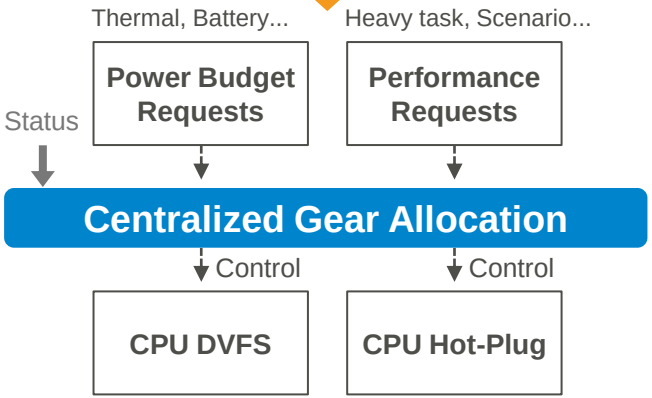
Previous Power Management

- Dynamic Voltage & Frequency Scaling (DVFS) and Hot-Plug drivers consider inputs separately:
  - Power budget, performance requests, and system status such as load, Thread Level Parallelism (TLP)
- Big gear on/off controlled by Hot-Plug driver



Centralized Gear Allocation

- A holistic control to handle increased complexity
- Tracking steady states to avoid unnecessary gear migration overhead
- Linking to user-specified performance, normal, power-saving modes

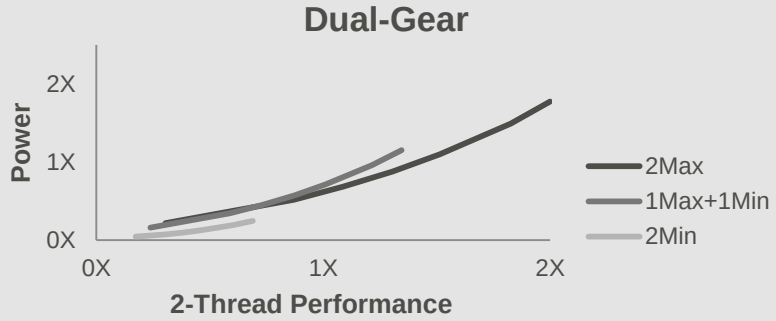


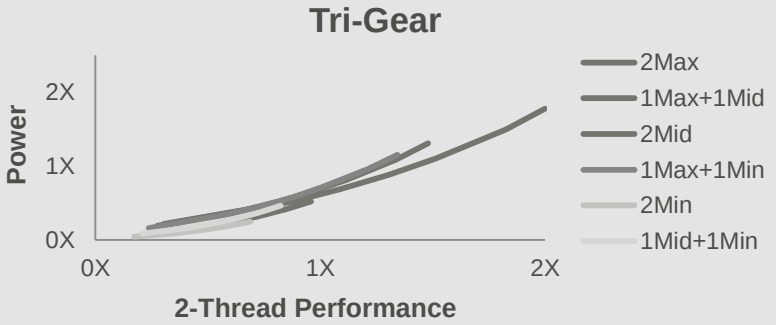
Adaptive Thermal Management (ATM)

Power budgeting by both core limit and frequency limit for all CPUs

Dual-Gear to Tri-Gear

- More possible solutions from core / frequency combination meeting power target
- 1.5X ~ 3X more possible solutions on core combination alone, depending on TLP





** Power and performance are relative to the highest point of Max curve*

** Each point in a curve represents a choice of gear / core / freq*

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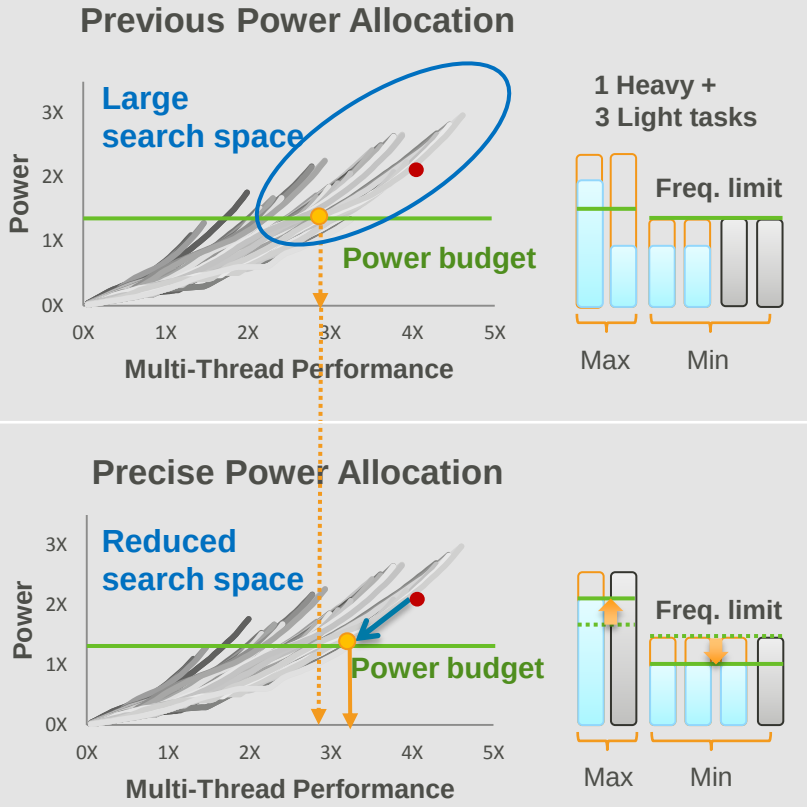
ATM for More Combinations

Previous power allocation

- Simple cost function: power efficiency only
- Large search space: chosen solution might not meet actual system requirement

Precise power allocation

- Comprehensive cost function: power efficiency, system requirement (#core, frequency and power), system overhead
- +10% Performance from considering **system requirement**
- -5˚C max Tj from reducing **system overhead**: hot-plug vs. DVFS latency



** Power and performance are relative to the highest point of Max curve*

** Geekbench v3 Multi-core Performance*

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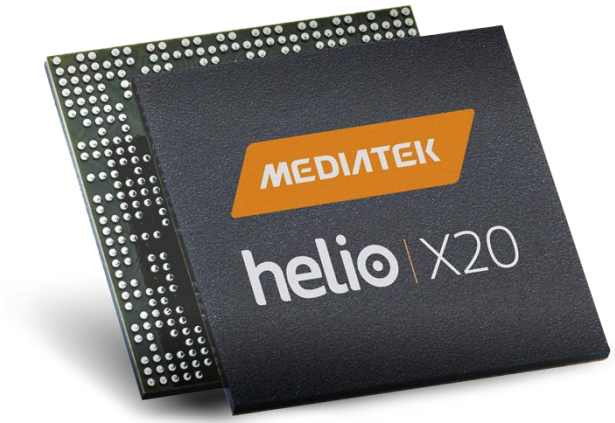
Agenda



Tri-Gear Concept

Challenges

Key Technologies

- Tailored CPU cores for gears
- Enhanced coherent interconnect
- Hybrid scheduler
- Holistic gear allocation
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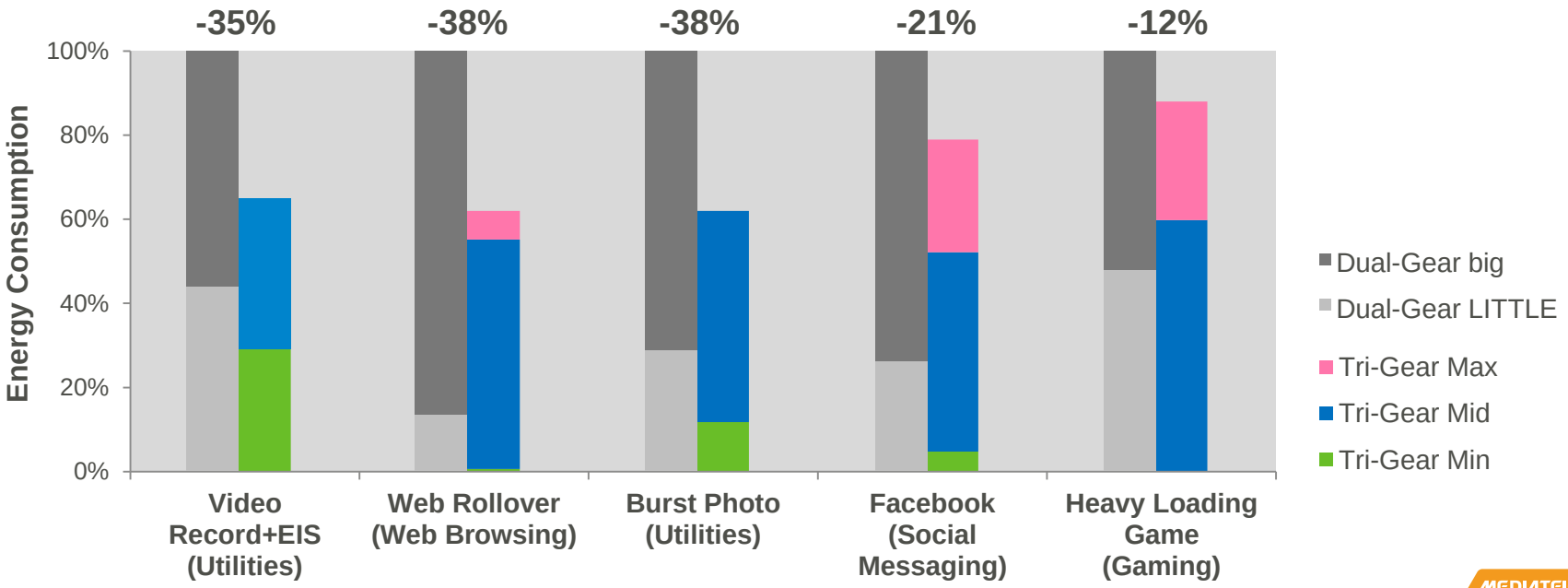
Achievements

Summary

Energy Saving from Tri-Gear CPU Architecture

Energy saving from Dual-Gear to Tri-Gear

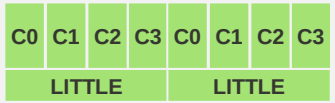
- Up to **-38%** CPU energy measured for scenarios used daily



CorePilot™ Technology Evolvement

SMP

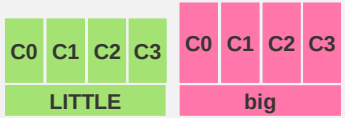
Symmetric Multi-Processing



MT6592

HMP

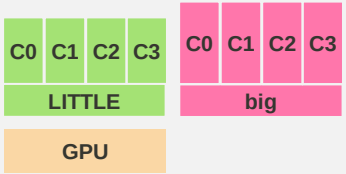
Heterogeneous Multi-Processing



MT6595

HC

Heterogeneous Computing



Helio P10

Tri-Gear

Hybrid Tri-Gear Multi-Processing

Helio X20

CorePilot™ 1.0		CorePilot™ 2.0	CorePilot™ 3.0
• Octa-core with SMP	• big.LITTLE HMP • Global Task Scheduling	• CPU+GPU Computing • Dynamic Gear Migration for low power	• **Tri-Gear** CPU Architecture • **12% ~ 38%** CPU energy saving

Summary

Majority of tasks are medium and light loads

- Added Mid gear and enhanced Min gear

CorePilot™ 3.0 Key Technologies

- Tailored CPU cores for gears
- Enhanced coherent interconnect
- Hybrid scheduler
- Holistic gear allocation
- Adaptive thermal management

Benefit of Tri-Gear

- Up to 38% CPU energy saving for typical scenarios used daily over extended performance range